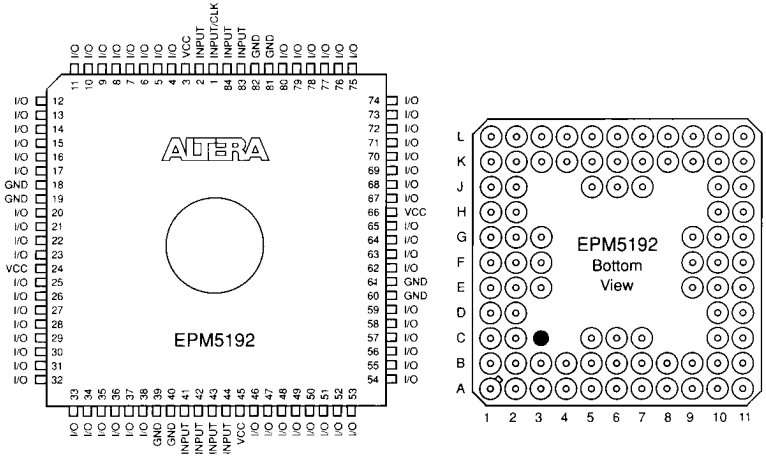
Features

- High-density, 192 macrocell, general-purpose MAX 5000 EPLD, easily integrating complete logic boards into a single package
- High-speed multi-LAB architecture
  - t_{PD} as fast as 25 ns
  - Counter frequencies up to 50 MHz
  - Pipelined data rates up to 62.5 MHz
- 384 shareable expander product terms ("expanders") offering flexibility for register and combinatorial logic expansion
- Programmable I/O architecture allowing up to 72 inputs or 64 outputs, and I/O tri-state buffers that facilitate connections to system buses
- Available in 84-pin windowed ceramic and plastic one-time-programmable (OTP) packages (see Figure 25):
  - J-lead chip carrier (JLCC and PLCC)
  - Pin-grid array (ceramic PGA only)

Figure 25. EPM5192 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Table 7 and 8 in this data sheet for pin-out information. Windows in ceramic packages only.



84-Pin J-Lead

84-Pin PGA

General Description

The Altera EPM5192 is a user-configurable, high-performance MAX 5000 EPLD that provides a high-density replacement for 74-series SSI and MSI TTL and CMOS logic. It can replace over 100 TTL SSI and MSI components and integrate the logic of over 20 22V10 devices. The EPM5192 consists of 192 macrocells equally divided into 12 Logic Array Blocks (LABs), each with 16 macrocells and 32 expanders. These compact LABs maintain high performance and efficient use of device resources. The EPM5192 has 8 dedicated input pins, one of which can be used as a global Clock. It can mix global and array clocking, facilitating easy integration of multiple subsystems. The EPM5192 contains 64 I/O pins that can be configured for input, output, or bidirectional operation, providing an interface to high-speed, bus-oriented applications. See Figure 26.

Figure 26. EPM5192 Block Diagram

Numbers without parentheses are for J-lead packages. Numbers in parentheses are for PGA packages. Numbers in brackets are for EPM5192A QFP packages.

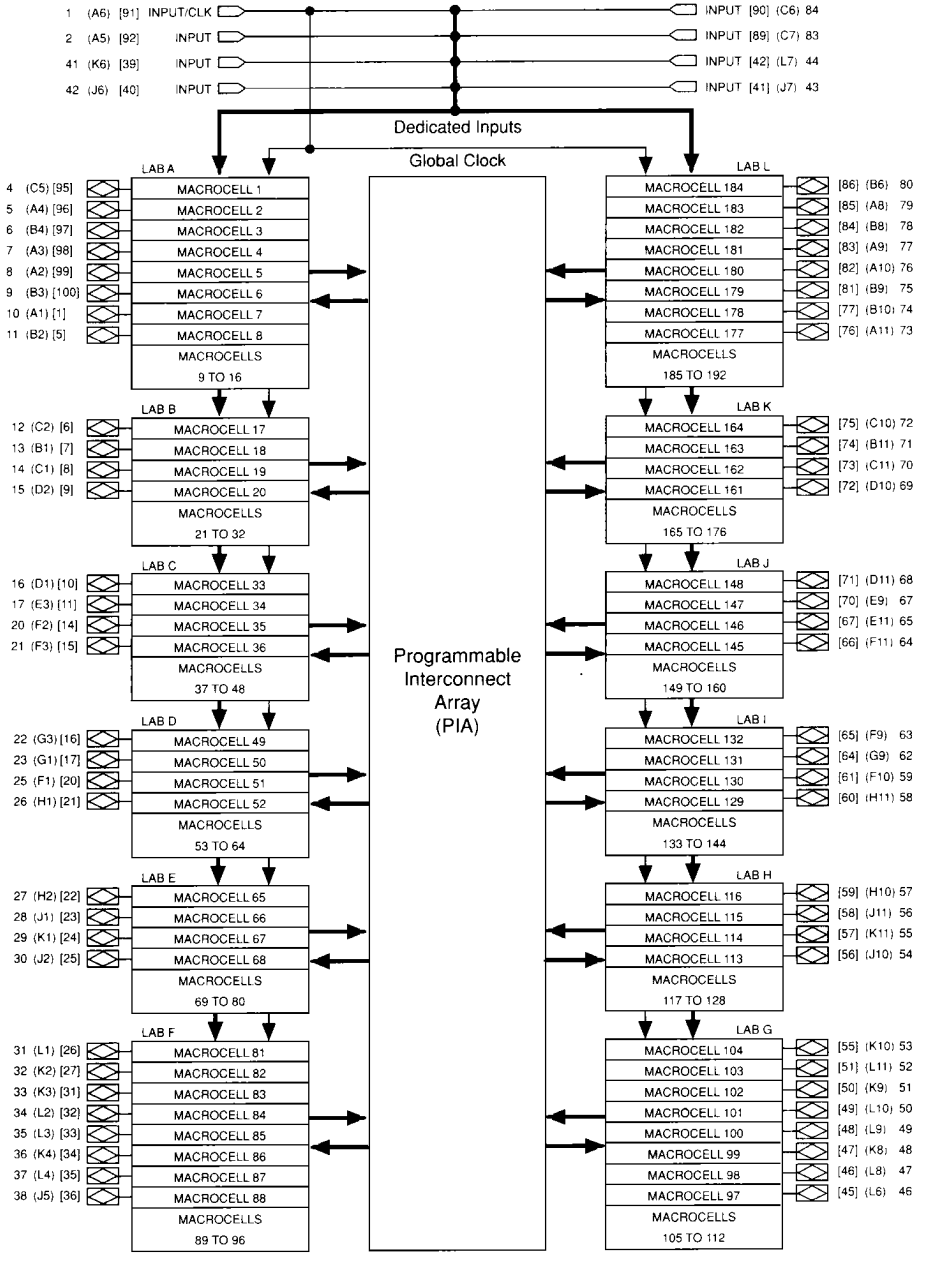
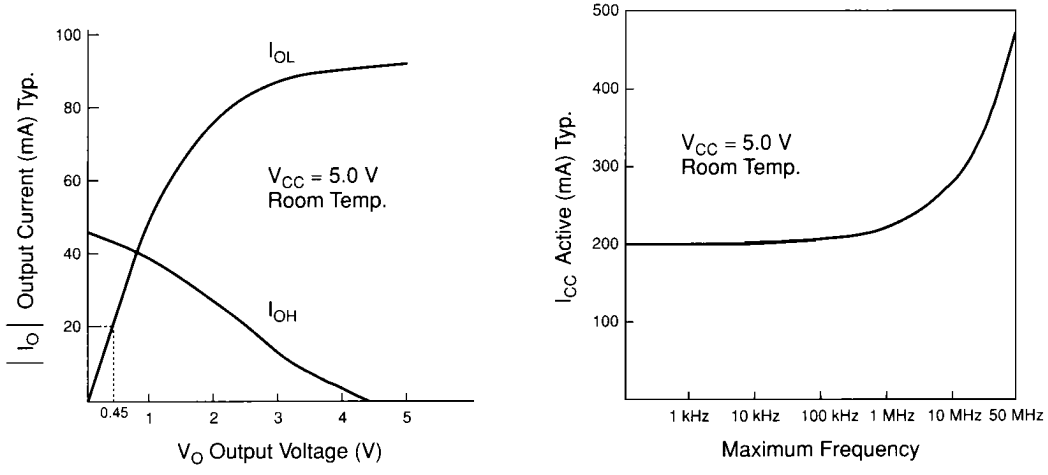


Figure 27 shows the output drive characteristics of EPM5192 I/O pins and typical supply current (I_{CC}) versus frequency for the EPM5192.

Figure 27. EPM5192 Maximum Output Drive Characteristics & I_{CC} vs. Frequency



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias, *Note (2)*	–65 [–55]	135 [125]	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Note (3)*	4.75 (5.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions *Notes (4), (5)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	*Note (2)*	2.0 [2.2]		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, *Notes (3), (6)*		250	360 (435)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *Notes (3), (6)*		270	380 (480)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (5)*

External Timing Parameters			EPM5192-1		EPM5192-2		EPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output			40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		10		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*Note (7)*	11		14		16		ns
t_{ACL}	Array clock low time		9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*Note (6)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*Note (6)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*Note (8)*	62.5		50		40		MHz

Internal Timing Parameters *Note (9)*			EPM5192-1		EPM5192-2		EPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		11	ns
t_{IO}	I/O input pad and buffer delay			6		6		11	ns
t_{EXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		14	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay			10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		12		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		4		6		8		ns
t_{IC}	Array clock delay			14		16		16	ns
t_{ICS}	Global clock delay			3		2		1	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in brackets are for MIL-STD-883-compliant versions only.
(3) Numbers in parentheses are for military- and industrial-temperature-range versions, as well as for MIL-STD-883-compliant versions.
(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(6) Measured with a 16-bit counter programmed into each LAB. I_{CC} measured at 0° C.
(7) This parameter is measured with a positive-edge-triggered Clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(8) The f_{MAX} values represent the highest frequency for pipelined data.
(9) For information on internal timing parameters, refer to *Application Brief 100 (Understanding EPLD Timing)* in this data book.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM5192-1, EPM5192-2, EPM5192
Industrial Temp.	(–40° C to 85° C)	EPM5192
Military Temp.	(–55° C to 125° C)	EPM5192
MIL-STD-883-Compliant	*Note (1)*	See *Military Products* in this data book.

Note:

(1) MIL-STD-883-compliant product specifications are provided in this data book and in Military Product Drawings (MPDs). However, only MPDs should be used to prepare Source Control Drawings (SCDs). MPDs are available from Altera Marketing at (408) 894-7000.

Pin-Out Information

Tables 7 and 8 provide pin-out information for the EPM5192.

Table 7. EPM5192 Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	84-Pin PGA
INPUT/CLK	1	A6
INPUT	2, 41, 42, 43, 44, 83, 84	A5, K6, J6, J7, L7, C7, C6
GND	18, 19, 39, 40, 60, 61, 81, 82	A7, B7, E1, E2, G10, G11, K5, L5
VCC	3, 24, 45, 66	B5, E10, G2, K7

Table 8. EPM5192 I/O Pin-Outs (Part 1 of 2)

MC	LAB	84-Pin J-Lead	84-Pin PGA	MC	LAB	84-Pin J-Lead	84-Pin PGA	MC	LAB	84-Pin J-Lead	84-Pin PGA
1	A	4	C5	17	B	12	C2	33	C	16	D1
2	A	5	A4	18	B	13	B1	34	C	17	E3
3	A	6	B4	19	B	14	C1	35	C	20	F2
4	A	7	A3	20	B	15	D2	36	C	21	F3
5	A	8	A2	21	B	–	–	37	C	–	–
6	A	9	B3	22	B	–	–	38	C	–	–
7	A	10	A1	23	B	–	–	39	C	–	–
8	A	11	B2	24	B	–	–	40	C	–	–
9	A	–	–	25	B	–	–	41	C	–	–
10	A	–	–	26	B	–	–	42	C	–	–
11	A	–	–	27	B	–	–	43	C	–	–
12	A	–	–	28	B	–	–	44	C	–	–
13	A	–	–	29	B	–	–	45	C	–	–
14	A	–	–	30	B	–	–	46	C	–	–
15	A	–	–	31	B	–	–	47	C	–	–
16	A	–	–	32	B	–	–	48	C	–	–
49	D	22	G3	65	E	27	H2	81	F	31	L1
50	D	23	G1	66	E	28	J1	82	F	32	K2
51	D	25	F1	67	E	29	K1	83	F	33	K3
52	D	26	H1	68	E	30	J2	84	F	34	L2
53	D	–	–	69	E	–	–	85	F	35	L3
54	D	–	–	70	E	–	–	86	F	36	K4
55	D	–	–	71	E	–	–	87	F	37	L4
56	D	–	–	72	E	–	–	88	F	38	J5
57	D	–	–	73	E	–	–	89	F	–	–
58	D	–	–	74	E	–	–	90	F	–	–
59	D	–	–	75	E	–	–	91	F	–	–
60	D	–	–	76	E	–	–	92	F	–	–
61	D	–	–	77	E	–	–	93	F	–	–
62	D	–	–	78	E	–	–	94	F	–	–
63	D	–	–	79	E	–	–	95	F	–	–
64	D	–	–	80	E	–	–	96	F	–	–

Table 8. EPM5192 I/O Pin-Outs (Part 2 of 2)

MC	LAB	84-Pin J-Lead	84-Pin PGA	MC	LAB	84-Pin J-Lead	84-Pin PGA	MC	LAB	84-Pin J-Lead	84-Pin PGA
97	G	46	L6	113	H	54	J10	129	I	58	H11
98	G	47	L8	114	H	55	K11	130	I	59	F10
99	G	48	K8	115	H	56	J11	131	I	62	G9
100	G	49	L9	116	H	57	H10	132	I	63	F9
101	G	50	L10	117	H	–	–	133	I	–	–
102	G	51	K9	118	H	–	–	134	I	–	–
103	G	52	L11	119	H	–	–	135	I	–	–
104	G	53	K10	120	H	–	–	136	I	–	–
105	G	–	–	121	H	–	–	137	I	–	–
106	G	–	–	122	H	–	–	138	I	–	–
107	G	–	–	123	H	–	–	139	I	–	–
108	G	–	–	124	H	–	–	140	I	–	–
109	G	–	–	125	H	–	–	141	I	–	–
110	G	–	–	126	H	–	–	142	I	–	–
111	G	–	–	127	H	–	–	143	I	–	–
112	G	–	–	128	H	–	–	144	I	–	–
145	J	64	F11	161	K	69	D10	177	L	73	A11
146	J	65	E11	162	K	70	C11	178	L	74	B10
147	J	67	E9	163	K	71	B11	179	L	75	B9
148	J	68	D11	164	K	72	C10	180	L	76	A10
149	J	–	–	165	K	–	–	181	L	77	A9
150	J	–	–	166	K	–	–	182	L	78	B8
151	J	–	–	167	K	–	–	183	L	79	A8
152	J	–	–	168	K	–	–	184	L	80	B6
153	J	–	–	169	K	–	–	185	L	–	–
154	J	–	–	170	K	–	–	186	L	–	–
155	J	–	–	171	K	–	–	187	L	–	–
156	J	–	–	172	K	–	–	188	L	–	–
157	J	–	–	173	K	–	–	189	L	–	–
158	J	–	–	174	K	–	–	190	L	–	–
159	J	–	–	175	K	–	–	191	L	–	–
160	J	–	–	176	K	–	–	192	L	–	–